CLAIMS

What is claimed is:

1. A method for providing a memory system design, comprising the steps of:

(a) receiving memory system criteria; and

(b) automatically extracting at least one memory system design based upon the memory system criteria.

2. The method of claim 1, wherein the receiving step (a) comprises:

(a1) providing a user interface; and

(a2) receiving the memory system criteria via the user interface.

3. The method of claim 1, wherein the memory system criteria comprises:

technical criteria; and

market criteria.

4. The method of claim 1, wherein the automatically extracting step (b) comprises:

(b1) automatically processing the memory system criteria; and

(b2) automatically extracting the at least one memory system design, wherein the at least one memory system design addresses the processed memory system criteria.

5. The method of claim 4, wherein the automatically extracting step (b2)

comprises:

(b2i) selecting a library type of multiple memory type modules based upon the memory system criteria;

(b2ii) selecting a family of multiple memory type modules in the library type based upon the memory system criteria;

(b2iii) selecting at least one of a memory device of one of a plurality of memory device types based upon the memory system criteria, wherein the memory system criteria comprises a choice of the plurality of memory device types;

(b2iv) computing a construction for a multiple memory type module for the one of the plurality of memory device types based upon the memory system criteria;

(b2v) computing an architecture for a multiple memory type module for the one of the plurality of memory device types based upon the memory system criteria;

(b2vi) repeating steps (b2iii) through (b2v) for each of the plurality of memory device types; and

(b2vii) determining a multiple memory type module in the family which comprises the plurality of memory type devices, the computed construction, and the computed architecture for each of the memory system criteria.

6. The method of claim 5, further comprising:

(b2viii) creating a design for a new multiple memory type module if the determined multiple memory type module does not exist in at least one library of multiple memory type modules.

7. The method of claim 1, further comprising:

(c) displaying the at least one memory system design.

8. The method of claim 1, wherein the at least one memory system design comprises a multiple memory type module.

9. The method of claim 8, wherein the multiple memory type module is comprised in at least one library, the at least one library comprising a plurality of multiple memory type modules.

10. The method of claim 9, wherein the plurality of multiple memory type modules comprises different combinations of memory types, architectures, data bus widths, banking schemes, or performance and power characteristics.

11. The method of claim 8, wherein the multiple memory type module comprises:

a plurality of memory devices, comprising:

at least one of a first memory device of a first memory type, and

at least one of a second memory device of a second memory type,

wherein a minimum configuration of the plurality of memory devices consists of:

one memory device of the first memory type, and

one or two memory devices of the second memory type; and

a single memory bus coupled to the plurality of memory devices, wherein the single

memory bus provides communication between a processor and the plurality of memory devices.

12. The method of claim 11, wherein neither the first memory device nor the second memory device stores an identification data describing a device composition of the memory module.

13. The method of claim 12, wherein the plurality of memory devices further comprises:

at least one of a third memory device of a third memory type, wherein the third memory device stores the identification data describing the device composition of the memory module.

14. The method of claim 11, wherein the single memory bus comprises:

a primary channel for communicating an operating system data from the plurality of memory devices to the processor;

an identification channel for communicating an identification data from the plurality of memory devices to the processor; and

a programming channel for providing programming and control signals necessary to program at least one of the plurality of memory devices.

15. The method of claim 14, wherein the programming channel comprises:

a dedicated sub-channel; and

one or more dual function sub-channel lines configured to communicate a programming signal to the plurality of memory devices when the single memory bus is in a programming mode, and to communicate a data transfer signal to the plurality of memory devices when the single memory bus operates in a data transfer mode.

16. The method of claim 14, wherein the single memory bus further comprises:

an expansion channel for communicating data between an additional memory device and the processor.

17. A system, comprising:

at least one library of multiple memory type modules, wherein the at least one library comprises:

a single memory bus;

a plurality of multiple memory type modules, wherein each of the plurality of multiple memory-type modules uses the single memory bus to communicate with a processor, wherein each of the plurality of multiple memory type modules comprises at least one of a first memory device of a first memory type and at least one of a second memory device of a second memory type; and

a computer readable medium coupled to the at least one library, wherein the computer readable medium comprises program instructions for automatically providing a memory system design, the instructions for:

(a) receiving memory system criteria, and

(b) automatically extracting at least one memory system design from the at least one library based upon the memory system criteria.

18. The system of claim 17, further comprising:

a user interface coupled to the computer readable medium for receiving the memory system criteria.

19. The system of claim 17, wherein the memory system criteria comprises:

technical criteria; and

market criteria.

20. The system of claim 17, wherein the automatically extracting instruction (b) comprises instructions for:

(b1) automatically processing the memory system criteria; and

(b2) automatically extracting the at least one memory system design from the at least one library, wherein the at least one memory system design address the processed memory system criteria.

21. The system of claim 20, wherein the automatically extracting instruction (b2) comprises instructions for:

(b2i) selecting a library type of multiple memory type modules based upon the

memory system criteria;

(b2ii) selecting a family of multiple memory type modules in the library type based upon the memory system criteria;

(b2iii) selecting at least one of a memory device of one of a plurality of memory device types based upon the memory system criteria, wherein the memory system criteria comprises a choice of the plurality of memory device types;

(b2iv) computing a construction for a multiple memory type module for the one of the plurality of memory device types based upon the memory system criteria;

(b2v) computing an architecture for a multiple memory type module for the one of the plurality of memory device types based upon the memory system criteria;

(b2vi) repeating steps (b2iii) through (b2v) for each of the plurality of memory device types; and

(b2vii) determining a multiple memory type module in the family which comprises the plurality of memory type devices, the computed construction, and the computed architecture for each of the memory system criteria.

22. The system of claim 21, further comprising:

(b2viii) creating a design for a new multiple memory type module if the determined multiple memory type module does not exist in at least one library of multiple memory type modules.

23. The system of claim 17, wherein the computer readable medium further

comprises the instructions for:

(c) displaying the at least one memory system design.

24. The system of claim 23, wherein the displaying instruction (c) comprises instructions for:

(c1) creating a new memory system design; and

(c2) displaying the new memory system design.

25. The system of claim 17, wherein a minimum configuration of each of the plurality of multiple memory type modules consists of:

one memory device of the first memory type, and

one or two memory devices of the second memory type.

26. The system of claim 25, wherein neither the first memory device nor the second memory device stores an identification data describing a device composition of the memory module.

27. The system of claim 26, wherein the plurality of memory devices further comprises:

at least one of a third memory device of a third memory type, wherein the third memory device stores the identification data describing the device composition of the memory module.

28. The system of claim 17, wherein the plurality of multiple memory type modules comprise different combinations of memory types, architectures, data bus widths, banking schemes, or performance and power characteristics.

29. The system of claim 17, wherein the single memory bus comprises:

a primary channel for communicating an operating system data from one of the plurality of multiple memory type modules to the processor;

an identification channel for communicating an identification data from one of the plurality of multiple memory type modules to the processor; and

a programming channel for providing programming and control signals necessary to program at least one memory device in one of the plurality of multiple memory type modules.

30. The system of claim 29, wherein the programming channel comprises:

a dedicated sub-channel; and

one or more dual function sub-channel lines configured to communicate a programming signal to one of the plurality of multiple memory type modules when the single memory bus is in a programming mode, and to communicate a data transfer signal to one of the plurality of multiple memory type modules when the single memory bus operates in a data transfer mode.

31. The system of claim 29, wherein the single memory bus further comprises:

an expansion channel for communicating data between an additional memory device and the processor.

32. A method for providing a memory system design, comprising the steps of:

(a) receiving memory system criteria;

(b) automatically processing the memory system criteria; and

(c) automatically extracting at least one memory system design, wherein the at least one memory system design comprises a multiple memory type module, wherein the multiple memory type module addresses the processed memory system criteria.

33. The method of claim 32, wherein the receiving step (a) comprises:

(a1) providing a user interface; and

(a2) receiving the memory system criteria via the user interface.

34. The method of claim 32, wherein the memory system criteria comprises:

technical criteria; and

market criteria.

35. The method of claim 32, wherein the multiple memory type module is comprised in at least one library, the at least one library comprising a plurality of multiple memory type modules.

36. The method of claim 35, wherein the plurality of multiple memory type modules comprise different combinations of memory types, architectures, data bus widths, banking schemes, or performance and power characteristics.

37. The method of claim 32, wherein the automatically extracting step (c) comprises:

(c1) selecting a library type of multiple memory type modules based upon the memory system criteria;

(c2) selecting a family of multiple memory type modules in the library type based upon the memory system criteria;

(c3) selecting at least one of a memory device of one of a plurality of memory device types based upon the memory system criteria, wherein the memory system criteria comprises a choice of the plurality of memory device types;

(c4) computing a construction for a multiple memory type module for the one of the plurality of memory device types based upon the memory system criteria;

(c5) computing an architecture for a multiple memory type module for the one of the plurality of memory device types based upon the memory system criteria;

(c6) repeating steps (c3) through (c5) for each of the plurality of memory device types; and

(c7) determining a multiple memory type module in the family which comprises the plurality of memory type devices, the computed construction, and the computed architecture for each of the memory system criteria.

38. The method of claim 37, further comprising:

(c8) creating a design for a new multiple memory type module if the determined multiple memory type module does not exist in at least one library of multiple memory type modules.

39. The method of claim 32, further comprising:

(d) displaying the at least one memory system design.

40. The method of claim 32, wherein the multiple memory type module comprises:

a plurality of memory devices, comprising:

at least one of a first memory device of a first memory type, and

at least one of a second memory device of a second memory type, wherein a minimum configuration of the plurality of memory devices consists of:

one memory device of the first memory type, and

one or two memory devices of the second memory type; and

a single memory bus coupled to the plurality of memory devices, wherein the single memory bus provides communication between a processor and the plurality of memory devices.

41. The method of claim 40, wherein neither the first memory device nor the second memory device stores an identification data describing a device composition of the

memory module.

42. The method of claim 41, wherein the plurality of memory devices further comprises:

at least one of a third memory device of a third memory type, wherein the third memory device stores the identification data describing the device composition of the memory module.

43. The method of claim 40, wherein the single memory bus comprises:

a primary channel for communicating an operating system data from the plurality of memory devices to the processor;

an identification channel for communicating an identification data from the plurality of memory devices to the processor; and

a programming channel for providing programming and control signals necessary to program at least one of the plurality of memory devices.

44. The method of claim 43, wherein the programming channel comprises:

a dedicated sub-channel; and

one or more dual function sub-channel lines configured to communicate a programming signal to the plurality of memory devices when the single memory bus is in a programming mode, and to communicate a data transfer signal to the plurality of memory devices when the single memory bus operates in a data transfer mode.

45. The method of claim 44, wherein the single memory bus further comprises:

an expansion channel for communicating data between an additional memory device and the processor.

46. A computer readable medium with program instructions for providing a memory system design, the instructions for:

(a) receiving memory system criteria; and

(b) automatically extracting at least one memory system design based upon the memory system criteria.

47. The medium of claim 46, wherein the receiving instruction (a) comprises instructions for:

(a1) providing a user interface; and

(a2) receiving the memory system criteria via the user interface.

48. The medium of claim 46, wherein the memory system criteria comprises:

technical criteria; and

market criteria.

49. The medium of claim 46, wherein the automatically extracting instruction (b) comprises instructions for:

(b1) automatically processing the memory system criteria; and

(b2) automatically extracting the at least one memory system design, wherein the at least one memory system design addresses the processed memory system criteria.

50. The medium of claim 49, wherein the automatically extracting instruction (b2) comprises instructions for:

(b2i) selecting a library type of multiple memory type modules based upon the memory system criteria;

(b2ii) selecting a family of multiple memory type modules in the library type based upon the memory system criteria;

(b2iii) selecting at least one of a memory device of one of a plurality of memory device types based upon the memory system criteria, wherein the memory system criteria comprises a choice of the plurality of memory device types;

(b2iv) computing a construction for a multiple memory type module for the one of the plurality of memory device types based upon the memory system criteria;

(b2v) computing an architecture for a multiple memory type module for the one of the plurality of memory device types based upon the memory system criteria;

(b2vi) repeating steps (b2iii) through (b2v) for each of the plurality of memory device types; and

(b2vii) determining a multiple memory type module in the family which comprises the plurality of memory type devices, the computed construction, and the computed architecture for each of the memory system criteria.

51. The medium of claim 50, further comprising instructions for:

(b2viii) creating a design for a new multiple memory type module if the determined multiple memory type module does not exist in at least one library of multiple memory type modules.

52. The medium of claim 46, further comprising instructions for:

(c) displaying the at least one memory system design.